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System and Method of Maintaining High Bandwidth
Requirement of a Data Pipe from Low Bandwidth Memories
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FIG. 1

Switch Bus **20**

Switch Bus **21**

14A scheduler

10A

DATAFLOW

EPC **12A**

EPC **12B**

10B

DATAFLOW

Data buffers **16B**

Data buffers **16A**

Ingress Bus **18**

WRAP

11

FAT PIPE **22**

14B scheduler

A

A

FIG. 2

Slice_0 (DDR DRAM)	Slice_1 (DDR DRAM)	Slice_2 (DDR DRAM)	Slice_3 (DDR DRAM)	Slice_4 (DDR DRAM)	Slice_N (DDR DRAM)

Scheduler Interface

DRAM Cntrl 0	DRAM Cntrl 1	DRAM Cntrl 2	DRAM Cntrl 3	DRAM Cntrl 4	DRAM Cntrl N

Scheduler Inf controller **32**

Memory arbiter **24**

R_request

26

Data_in

Receiver Controller

W_request

R/W request

Buffer acceptance & accounting **34**

Enq FCB

30

Transmitter Controller

Data_out

Lease/chain BCB

Lease/chain FCB

EPC interface Controller **28**

FCB arbiter

BCB arbiter

Release/dechainBCB&FCB

G-FIFO QDR SRAM

TP/TB QDR SRAM

BCB lists QDR SRAM

EPC interface

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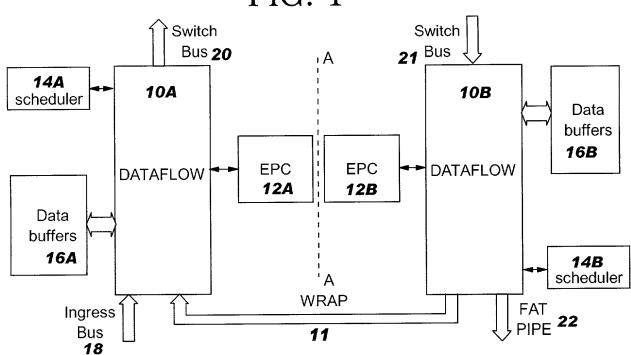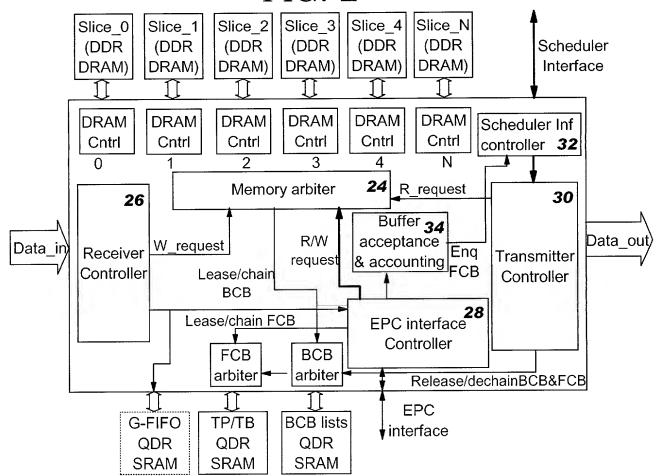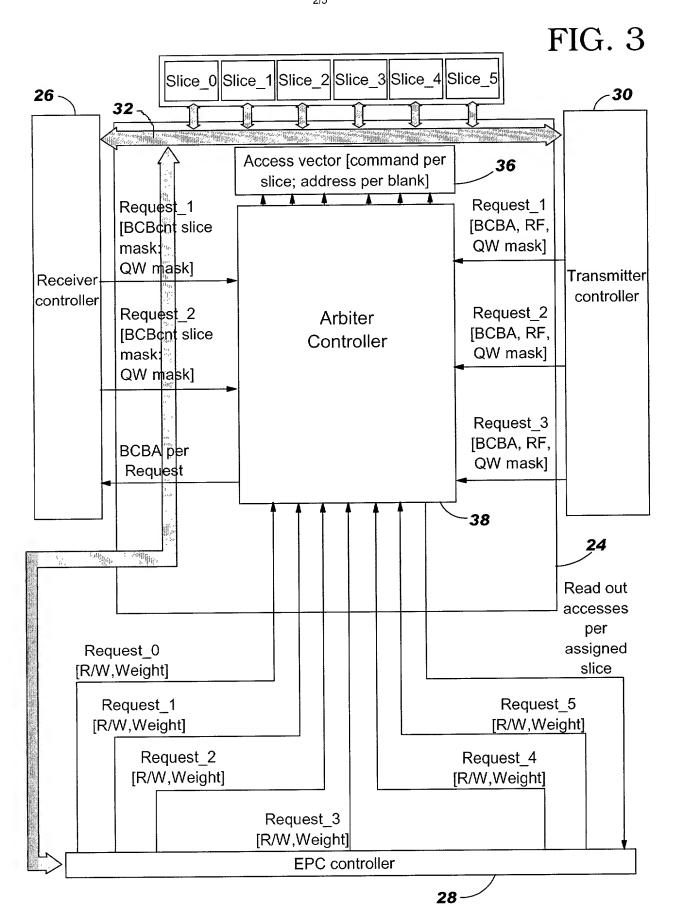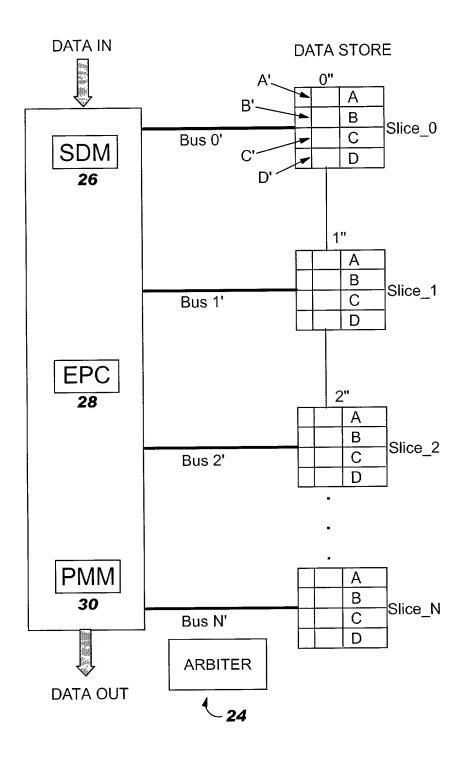Requirement of a Data Pipe from Low Bandwidth Memories
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FIG. 3

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FIG. 4

DATA IN

DATA STORE

SDM
26

Bus 0'

A'
B'
C'
D'

0"

	A
	B
	C
	D

Slice_0

1"

	A
	B
	C
	D

Slice_1

EPC
28

Bus 1'

2"

	A
	B
	C
	D

Slice_2

Bus 2'

.
.
.

PMM
30

Bus N'

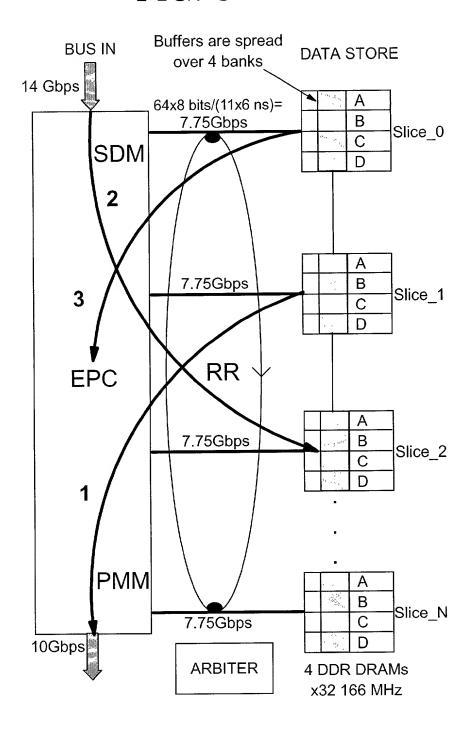| | A |
	B
	C
	D

Slice_N

DATA OUT

ARBITER

24

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FIG. 5

BUS IN

Buffers are spread over 4 banks

DATA STORE

14 Gbps

64×8 bits/$(11 \times 6$ ns$)=$ 7.75Gbps

SDM

2

7.75Gbps

	A
	B
	C
	D

Slice_0

3

7.75Gbps

	A
	B
	C
	D

Slice_1

EPC

RR

7.75Gbps

	A
	B
	C
	D

Slice_2

1

PMM

7.75Gbps

	A
	B
	C
	D

Slice_N

10Gbps

ARBITER

4 DDR DRAMs
x32 166 MHz

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FIG. 6